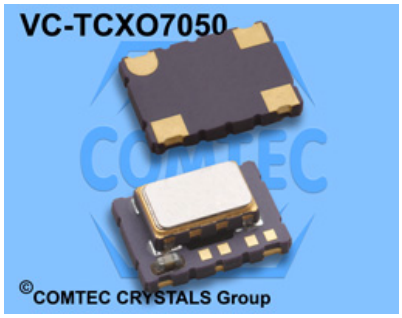
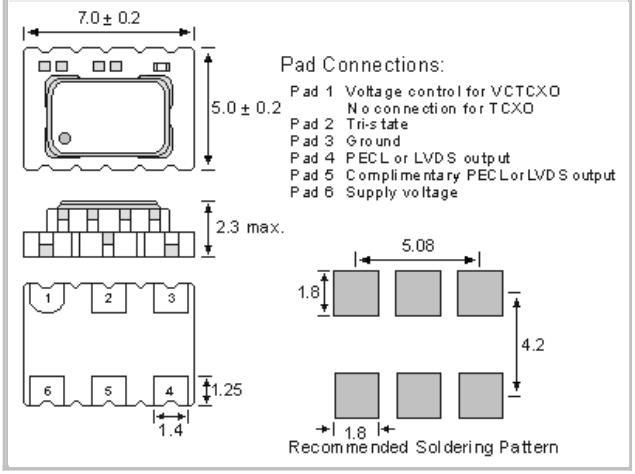



VC-TCXO Oscillator LVPECL Differential
VC-TCXO7050PW3.3 3.3V

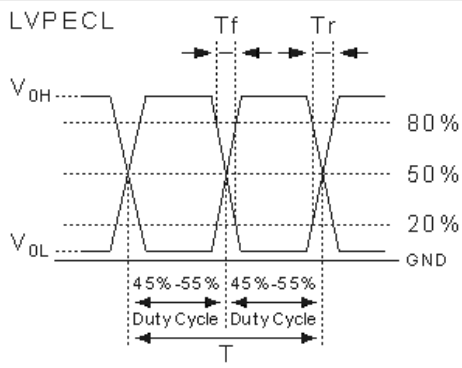
- SMD in ceramic case (7.0 x 5.0 x 2.3) mm
- LVPECL Square Wave Output Wave Form
- Low cost, low jitter
- RoHS conform; Lead-free product; Tape & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies

External Dimensions




RoHS COMPLIANT

LVPECL Square Wave Output Wave Form




## Specifications

| | |
|---|---|
| Holder Type: | VC-TCXO7050PW3.3 3.3V(Voltage code is "3.3"); Tri-State on pad 2 |
| Frequency Range: | 10.0 MHz ~ 800 MHz |
| Freq. Stability vs Temperature: | 0° to 50°C (±1.0ppm) to -40 to +85°C ( ±3.0 to ± 5.0ppm) |
| Freq. Stability vs Aging: | ± 1.0 ppm, first year at 25°C |
| Freq. Stability vs Voltage Change: | ± 0.3 ppm, for a ± 5% input voltage change |
| Freq. Stability vs Load Change: | ± 0.3 ppm, for a ± 10% load condition change |
| Current Consumption (max.): | 10MHz ≤ fout ≤ 25MHz: 65mA (max); 25MHz ≤ fout ≤ 100MHz: 85mA (max); 100MHz ≤ fout ≤ 800MHz: 115mA (max) |
| Output Symmetry (Duty Cycle): | 50% ± 5% measured at Vdd-1.3V |
| Output Load: | 50 Ohm to Vdd-2.0V / CL = 15pF |
| Output Logic Levels: | High"1"Voh=2.275V(min) Vdd-1.025min.,Condition: RL= 50 Ohm to (Vdd-2.0V)<br>Low"0"VoL=1.680V(max.) Vdd-1.620max.,Condition: RL= 50 Ohm to (Vdd-2.0V) |
| Rise/Fall Time: | 1.5ns max. @ 20% to 80% of PECL wave form |
| Start Up Time: | 5 ms (typ), 10.0ms (max.) (reach 90% amplitude and at+25°C ±2°C) |
| Pin 1 Options VCTCXO only: | Control Voltage Center, Range: +1.5V ± 1.0V<br>Frequency Deviation Range: ±5.0ppm(min.) with Vcon = +1.5V ±1.0V<br>Linearity: 6% typical ; 10% max.<br>Slope Polarity: Positive voltage for positivefrequency shift |
| Tri-state Funct. on Pin2, No Connection | Differential PECL and compliantary PECL outputs |
| Tri-state Function on Pin 2, Disable: | Both outputs are disabled (high impedance) when pad 2 is taken below 0.45*Vcc referenced to ground (threshold) Oscillator is always On. Only buffer stage is disabled. Disable current: 50µA mac. (at 0.0V), Disable time: 10ns (max.) |
| Tri-state Function on Pin 2, Enable: | At disabled mode , both outputs are enabled when Tri-state pad is taken above 0.45 Vcc referenced to ground (threshold);<br>Enable time: 10ns + one period of the output frequency (max.) |
| Phase Noise: | Offset 10Hz 100Hz 1kHz 10kHz 100kHz<br>155.520 MHz :-65dBc/Hz -95dBc/Hz -120dBc/Hz -125dBc/Hz -121dBc/Hz<br>622.080 MHz :-55dBc/Hz -85dBc/Hz -109dBc/Hz -115dBc/Hz -110dBc/Hz |
| Phase Jitter (RMS) (12 kHz to 20 MHz): | 2.6 ps typ., 4ps max., for 155.520MHz |
| Period Jitter (typical): | Frequency Range: 38.880MHz 77.760MHz 155.520MHz 622.080MHz<br>(RMS): 2.2ps 3.5ps 4.3ps 5.0ps<br>(Peak to peak) : 17.0ps 25.0ps 27.0ps 32.0ps |
| Temperature: | Storage Temp. -55°C to +125°C / Reflow Condition 260°C max for 10 sec. |

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