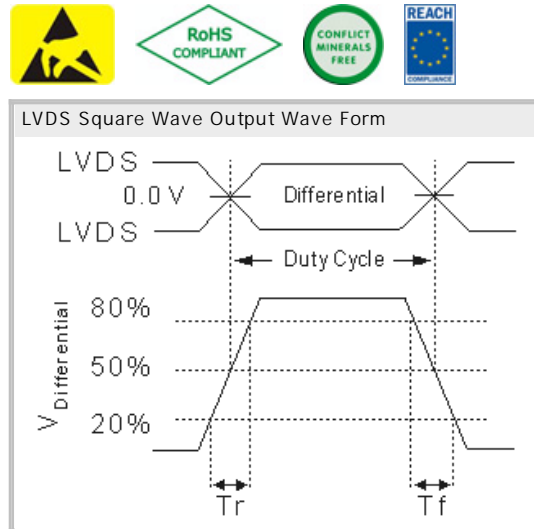
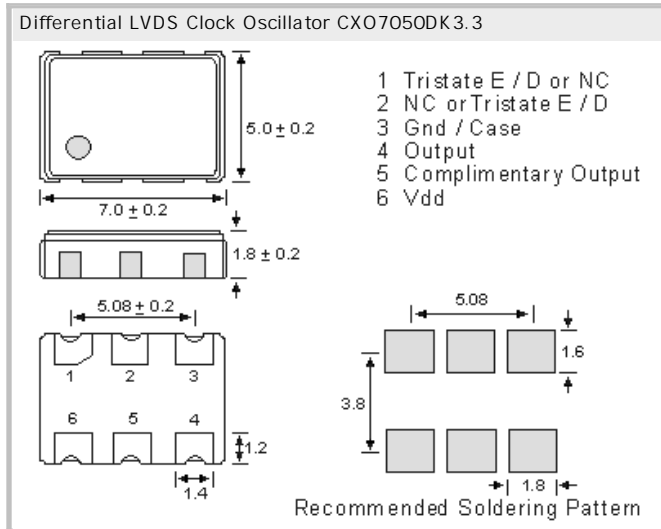


Differential LVDS Clock Oscillator
CXO7050DK3.3, 3.3V, 0.2ps Jitter, non PLL

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- Femto second integrated phase jitter (0.2ps typical, 12 KHz to 20 MHz)
- Superior phase noise (-138 dBc/Hz at 10 KHz and -142 dBc/Hz at 100 KHz offset)
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave



Specifications

Holder Type:	Differential LVDS Clock Oscillator CXO7050DK3.3; 3.3V; Tri-State on pad 1
Frequency Range:	13.500 MHz ~ 220.000 MHz
Frequency Stability at 25°C:	± 20 to ± 100 ppm
Operating Temperature Range:	-20° C to + 70° C, -40° C to + 85° C
Storage Temperature:	-50° C to + 100° C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 5%
Maximum Supply Current (15pF load):	16mA typica; I 27mA max.
Output Voltage Swing:	250 mV min. , 350 mV typ. , 450 mV max. , RL = 100 ,
Output Logic Levels:	High "1" 1.43V typical; 1.6V max, RL= 100 ohms.; Low "0" 0.9V min; 1.1V typical, RL= 100 ohms
Output Symmetry (Duty Cycle):	50% ± 5% max. measured at 50% waveform
Load:	RL= 100 between output and complimentary output
Rise/Fall Time:	Tr = 0.2 ns. typ; 0.4 ns. max. 20% -> 80% of waveform Tf = 0.2 ns. typ; 0.4 ns. max. 80% -> 20% of waveform
Start Up Time:	± 3 ppm max. first year ; ± 2 ppm max. per year thereafter
Tri-state Function Pin 1:	Enable II When 70% min. of VDD to Enable Output. Enable time : 10 ms max. Disable II When 30% max. of VDD to Disable Output. Disable current : 10 µA max. , Disable time : 0.2 µs max.
Phase Jitter (12 kHz to 20 MHz):	0.2 ps typical, 0.5 ps (max.), for 156.250 MHz, 3.3V
Phase Noise (156.250 MHz, 3.3V):	-50dBc/Hz @ 10Hz, -80dBc/Hz @ 100Hz, -115dBc/Hz @ 1kHz -135dBc/Hz @ 10kHz, -142dBc/Hz @ 100kHz, -147dBc/Hz @ 1MHz, -152dBc/Hz @ 10MHz
Aging:	< ± 3ppm max. for the first year
Reflow Condition:	260° C max for 10 sec.

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