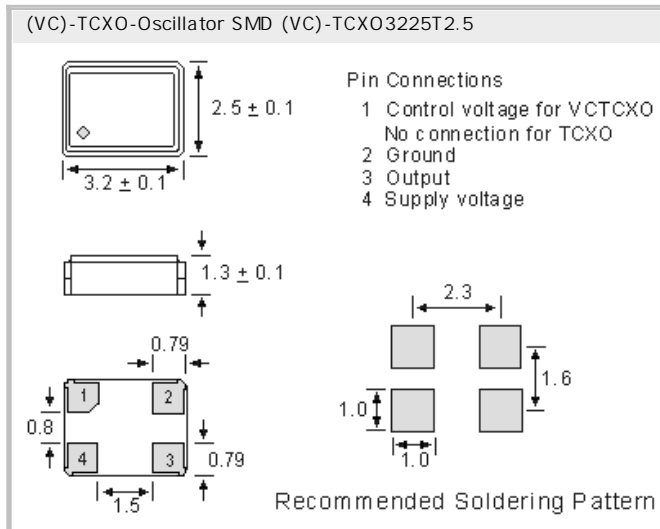
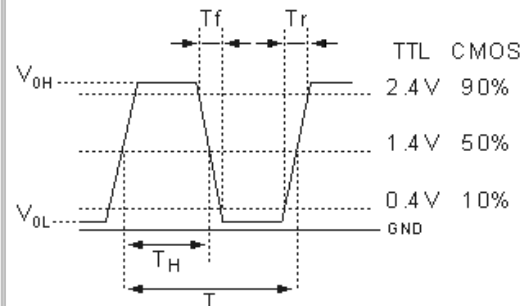


(VC)-TCXO-Oscillator SMD
(VC)-TCXO3225T2.5 2.5V CMOS/TTL

- Temperature Compensated Crystal Oscillators
- SMD in ceramic case (3.2 x 2.5 x 1.0) mm
- CMOS/TTL Square Wave Output;
Wave form code is " T "
- on Tape & Reel
- RoHS conform; Lead-free product



CMOS/TTL Output Wave Form



Specifications

Holder Type:	(VC)-TCXO3225T2.5 2.5V (Voltage code is " 2.5 ")
Frequency Range:	8.192 MHz to 40.0 MHz
Frequency Stability:	± 0.5ppm to ± 3.0ppm
Standard Frequencies (Part list):	10.0, 12.8, 13.0, 14.4, 15.36, 16.384, 19.2, 19.44, 19.68, 25.0, 20.0, 27.0, 38.88, 40.0
Freq. Stability vs Temperature:	0° to 50°C (± 0.5ppm) to -40 to + 85°C (± 1.0 to ± 3.0ppm)
Input Voltage:	+ 2.5V ± 10%
Freq. Stability vs Aging:	± 1.0 ppm, first year at 25 °C
Freq. Stability vs Voltage Change:	± 0.3 ppm, for a ± 5% input voltage change
Freq. Stability vs Load Change:	± 0.3 ppm, for a ± 10% load condition change
Current Consumption:	6mA (Freq. dependent)
Output Load:	15pF
Voltage Control on pin 1 (EFC):	Electronic Frequency Tuning (EFC) Optionally
Pin 1 Options VCTCXO only (EFC):	Control Voltage: Standard + 1.5V ± 1.0V for all input voltages. Slope Polarity: Positive slope. Positive voltage for positive frequency shift. Input Impedance: 50kOhm min.; Linearity ± 10% max. Modulation Bandwidth (at-3 dB) : 20kHz min.
Frequency Deviation Range (EFC):	± 5.0ppm (min.) with Vcon = + 1.5V ± 1.0V (Optionally)
Output Logic Levels:	Logic High "1" : 90% Vdd min. // Logic Low "0" : 10% Vdd min.
Output Symmetry (Duty Cycle):	40/60% normal, 45/55% tight at 50%
Rise/Fall Time CMOS:	10.0ns (max.) Measured between 20% and 80% Vdd of the wave form (CL = 15pF)
Start Up Time:	10 ms (max.); 5ms (typ.)
Phase Noise (10.00MHz 3.3V):	- 96dBc/Hz at 10Hz offset -122dBc/Hz at 100Hz offset -138dBc/Hz at 1kHz offset -145dBc/Hz at 10kHz offset -150dBc/Hz at 100kHz offset
Storage Temperature:	-55 to + 105°C
Reflow Condition:	260°C max. for 10 sec.

GERMANY:

COMTEC CRYSTALS GmbH · Sultenstrasse 12-14
8 5 5 8 6 P o i n g / G E R M A N Y
Phone +49 8121 778160 · Fax +49 8121 778177
e-Mail info@comtec-crystals.com
Internet: <http://www.comtec-crystals.com>
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FRANCE:

COMTEC CRYSTALS SARL · 23, rue du Faucon
6 7 5 0 0 H a g u e n a u / F R A N C E
Phone +33 388 732162 · Fax +33 388 730118
e-Mail sales@comtec-crystals.com
Internet: <http://www.comtec-crystals.com>
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