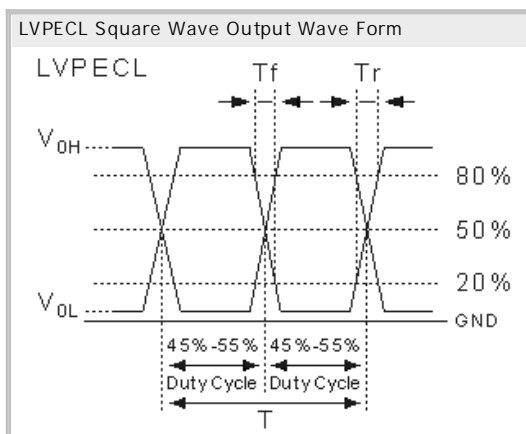
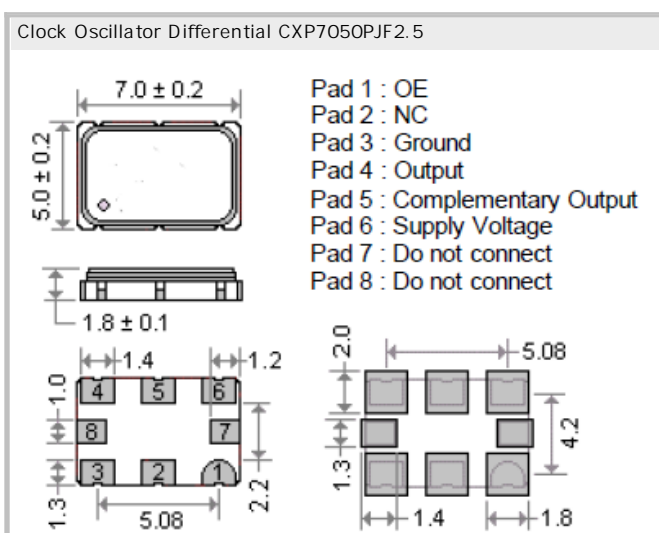




Clock Oscillator Differential CXP7050PJF2.5
LVPECL 2.5V; ultra low jitter, with PLL

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- LVPECL Differential Output Wave Form
- High Q fundamental crystal + ultra low jitter multiplier circuit
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies



Specifications

| | |
|--|---|
| Holder Type: | Clock Oscillator CXP7050PJF2.5 ; 2.5V (Voltage code is "2.5") |
| Frequency Range: | 150 MHz to 2.100.0 MHz |
| Frequency Stability at 25°C: | ± 25 ppm / ± 50 ppm |
| Operating Temperature Range: | ± 25 ppm, -40°C to +85°C / ± 50 ppm, -40°C to +85°C |
| Storage Temperature: | -55°C to +150°C |
| Power Supply Voltage (Vdd): | + 2.5V D.C. ± 10% |
| Maximum Supply Current (Differential): | 100mA typ. 120mAmax. |
| Current with Output Disabled: | 99 mA typical |
| Output Voltage (VOH) (VOL): | High "1" Vdd-1.165V min, Vdd- 0.8Vmax. Low "0" Vdd-2.0V min, Vdd- 1.55Vmax. |
| Output Voltage Swing: | 595 mV min., 930 mV max. |
| Start Up Time: | 5ms typical; 10 ms max. |
| Output Symmetry (Duty Cycle): | 50% ± 5% max. (measured at 50% Vdd) |
| Load: | 50 ohms into Vdd -2V or Thevenin equiv. |
| Output Enable / Disable: | 2.5ms max.; 10µs max.; (20% Vdd <-> 80% Vdd) |
| RMS Phase Jitter (12 kHz to 20 MHz): | 156.250 MHz: 159fs; 491.520MHz: 155fs; 644.530MHz: 151fs; 1.480MHz: 147fs; 2GHz: 163fs |
| Aging: | < ± 3ppm max. for the first year; ± 2ppm max. per years thereafter |
| Reflow Condition: | 260°C max for 10 sec. |

GERMANY:

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