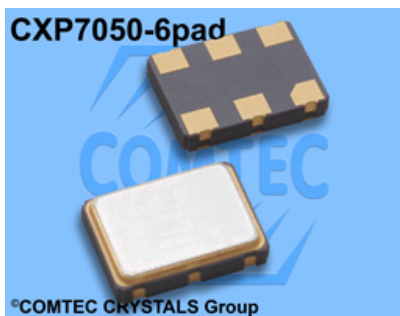
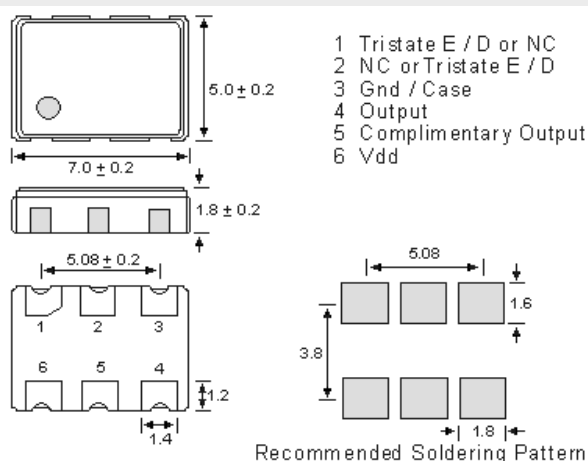




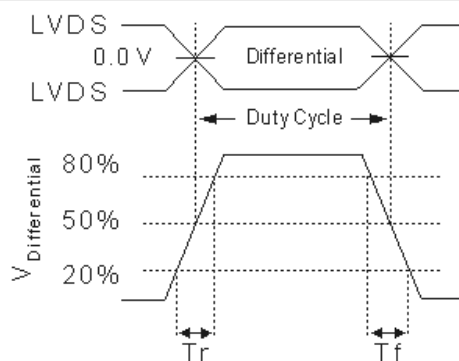
Clock Oscillator LVDS Differential  
CXP7050DQN3.3, 3.3V, 0,6ps typical Phase Jitter, with PLL

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- LVDS Square Wave Output Wave Form
- High Q fundamental crystal + low jitter multiplier circuit + ultra low jitter multiplier circuit
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies

Clock Oscillator LVDS, CXP7050DQN3.3



LVDS Square Wave Output Wave Form



## Specifications

|                                        |                                                                                                                                                                                              |
|----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Holder Type / Voltage (Vdd):           | CXP7050DQN3.3; + 3.3V D.C. ± 5%; Tri-State on pad 1                                                                                                                                          |
| Frequency Range:                       | 150.000 MHz to 1500.000 MHz                                                                                                                                                                  |
| Frequency Tolerance at 25°C:           | ±20 to ±100 ppm                                                                                                                                                                              |
| Operating-/Storage -Temperature Range: | -20°C to +70°C, -40°C to +85°C // -55°C to +150°C                                                                                                                                            |
| Maximum Supply Current (15pF load):    | 100MHz: 18mA typical to 1.35GHz: 28mA typical;                                                                                                                                               |
| Output Logic:                          | "High", 1: 1.4V (typical); 1.6V (max.), RL = 100 Ohm<br>"Low ", 0: 0.9V (min); 1.1V (typical), RL = 100 Ohm                                                                                  |
| Output Voltage Swing:                  | 250mV min., 350 typ., 450mV max., RL = 100 Ohm                                                                                                                                               |
| Load:                                  | 100 Ohm between output and complimentary output                                                                                                                                              |
| Rise (Tr)/Fall Time (Tf):              | 0.2ns typical; 0.5ns max. (20%Vdd<->80% of the LVDS wave form)                                                                                                                               |
| Start Up Time:                         | 5 ms typical; 10ms max.                                                                                                                                                                      |
| Tri-state Function Pin 1:              | Enable II When 70% min. of VDD to Enable Output. Enable time : 200 ns max.<br>Disable II When 30% max. of VDD to Disable Output.<br>Disable current : 16 mA max. , Disable time : 50 ns max. |
| Phase Jitter:                          | 0.6 ps typ. (12 kHz to 20 MHz); < 100 fs (1.875 MHz to 20MHz)                                                                                                                                |
| Phase Noise (156.250 MHz):             | -67dBc/Hz @ 10Hz, -92dBc/Hz @ 100Hz, -112dBc/Hz @ 1kHz<br>-121dBc/Hz @ 10kHz, -124dBc/Hz @ 100kHz, -136dBc/Hz @ 1MHz,<br>-153dBc/Hz @ 10MHz                                                  |
| Aging:                                 | < ±3ppm max. for the first year; ±2ppm max. per year thereafter                                                                                                                              |
| Reflow Condition:                      | 260°C max for 10 sec.                                                                                                                                                                        |

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