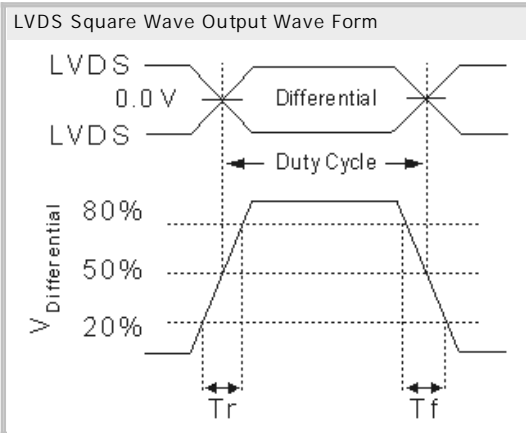
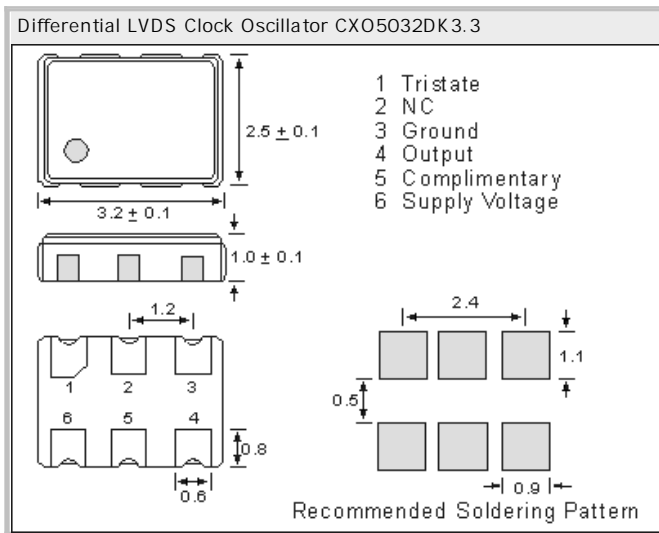


Differential LVDS Clock Oscillator  
CXO3225DK3.3, 3.3V, 0,2 psec Jitter, non PLL

- SMD in ceramic case (3.2 x 2.5 x 1.0) mm
- Tri-State Enable / Disable on pad No. 1
- Femto second integrated phase jitter (200 fs typical, 12 KHz to 20 MHz)
- Superior phase noise (-138 dBc/Hz at 10 KHz and -142 dBc/Hz at 100 KHz offset)
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- High performance with surprisingly low price



## Specifications - Product No. G100000000QTSUPN43AB

|                                     |  |
|-------------------------------------|--|
| Holder Type:                        | CXO3225DK3.3; 3.3V(Voltage code is "3.3"); Tri-State on pad 1  |
| Frequency:                          | 100.000000 MHz   |
| Frequency Stability at 25°C:        | ± 25.0 ppm   |
| Operating Temperature Range:        | ± 25.0 ppm ; -40°C to +85°C (inclusive of 25°C tolerance, ±10% input voltage variation, load change, aging, shock and vibration )  |
| Storage Temperature:                | -55°C to +150°C  |
| Power Supply Voltage (Vdd):         | + 3.3V D.C. ± 5%   |
| Maximum Supply Current (15pF load): | 16.0 mA typ.   |
| Output Voltage Swing:               | 250 mV min; 350 mV typical; 450 mV max. RL= 1000ohm  |
| Output Logic Levels:                | High "1" 1.43V typical; 1.6V max, RL= 100 ohms.;<br>Low "0" 0.9V min; 1.1V typical, RL= 100 ohms   |
| Output Symmetry (Duty Cycle):       | 50% ± 5% max. measured at 50% waveform   |
| Load:                               | RL= 100 ohms between output and complimentary output   |
| Rise/Fall Time:                     | Tr = 0.2 ns. typ; 0.4 ns. max. 20% -> 80% of waveform<br>Tf = 0.2 ns. typ; 0.4 ns. max. 80% -> 20% of waveform   |
| Start Up Time:                      | ± 3 ppm max. first year ; ± 2 ppm max. per year thereafter   |
| Tri-state Function Pin 1:           | Enable II When 70% min. of VDD to Enable Output. Enable time : 10 ms max.<br>Disable II When 30% max. of VDD to Disable Output.<br>Disable current : 10 µA max. , Disable time : 0.2 µs max. |
| Phase Jitter (12 kHz to 20 MHz):    | 0.2 ps typical, 0.5 ps (max.), for 156.250 MHz, 3.3V   |
| Phase Noise (156.250 MHz):          | -50dBc/Hz @ 10Hz, -80dBc/Hz @ 100Hz, -115dBc/Hz @ 1kHz<br>-135dBc/Hz @ 10kHz, -142dBc/Hz @ 100kHz, -147dBc/Hz @ 1MHz,<br>-152dBc/Hz @ 10MHz  |
| Aging:                              | < ± 3ppm max. for the first year   |
| Reflow Condition:                   | 260°C max for 10 sec.  |

### GERMANY:

COMTEC CRYSTALS GmbH · Sultenstrasse 12-14  
8 5 5 8 6 P o i n g / G E R M A N Y  
Phone +49 8121 778160 · Fax +49 8121 778177  
e-Mail [info@comtec-crystals.com](mailto:info@comtec-crystals.com)  
Internet: <http://www.comtec-crystals.com>  
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### FRANCE:

COMTEC CRYSTALS SARL · 23, rue du Faucon  
6 7 5 0 0 H a g u e n a u / F R A N C E  
Phone +33 388 732162 · Fax +33 388 730118  
e-Mail [sales@comtec-crystals.com](mailto:sales@comtec-crystals.com)  
Internet: <http://www.comtec-crystals.com>  
Sous réserve de modifications.