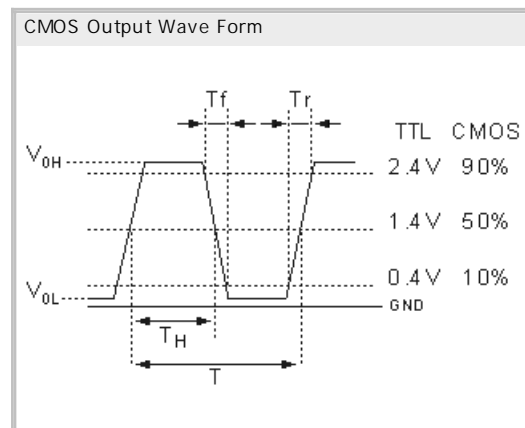
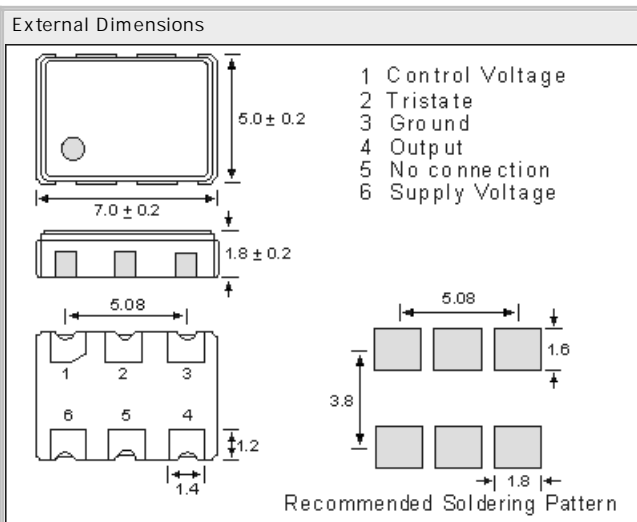


Clock Oscillator VCXO7050TV3.3-6pad, 3.3V
Voltage Controlled Crystal Oscillators

- CMOS/TTL Output Wave Form
- SMD in ceramic case (7.0 x 5.0 x 1.8) mm, on Tape & Reel (Tape 16mm)
- with Tri-State Function, 3.3 V
- High Q fundamental crystal + low jitter multiplier circuit
- RoHS conform; Lead-free product
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 100GG 1/2 sine wave
- Available in many standard and special frequencies



Specifications

Holder Type:	VCXO7050TV3.3-6pad, 3.3V(Voltage code is "3.3"); Tri-State
Frequency Range:	50 MHz to 200.0 MHz
Frequency Stability at 25°C:	± 25ppm (typ.) , ± 50ppm, ± 100ppm
Frequency Deviation:	± 80ppm min.
Initial Freq. Accuracy (at 25 °C):	To tune to the nominal frequency with $V_c = 1.65V \pm 0.15V$
Operating Temperature Range:	-20°C to +70°C, -40°C to +85°C
Storage Temperature:	-50°C to +150°C
Power Supply Voltage (Vdd):	+ 3.3V D.C. ± 5%
Maximum Supply Current (15pF load):	12 - 200 MHz 40mA (max.)
Voltage Control:	1.65V DC Center / 0.3V to 3.0V Range
Load:	15 pF
Output Logic Levels:	High "1" 90% of Vdd-min, Low "0" 10% Vdd-max.,
Output Symmetry (Duty Cycle):	50% ± 5% max. (measured at 50% Vdd)
Modulation Bandwidth (at -3 dB):	25KHz min. 0V Vcontrol 3.3V
Rise/Fall Time:	2.4ns typical, (0.3V<-> 3.0V, 15pF load)
Linearity:	6% typical, 10% max.
Start Up Time:	10 ms (max.); 5 ms (typical)
Tri-State Function:	Tri-State Enable High. No connection or 70% of Vdd min. is applied to a Tri-state pad to enable output. 30% of Vddmax. to disable outputs (high impedance).
Phase Jitter (12 kHz to 20 MHz):	2.3 ps typ., 4.0pS (max.) for 155.520MHz
Phase Noise (typical), Vcon : GND:	(Offset 155.520 MHz) -65dBc/Hz @ 10Hz, -95dBc/Hz @ 100Hz, -120dBc/Hz @ 1kHz -125dBc/Hz @ 10kHz, -121dBc/Hz @ 100kHz, -120dBc/Hz @ 1MHz
Aging:	< ± 3ppm max. for the first year; 2ppm max. per year thereafter
Input Impedance:	2 MOhm (min.)
Reflow Condition:	260°C max for 10 sec.

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