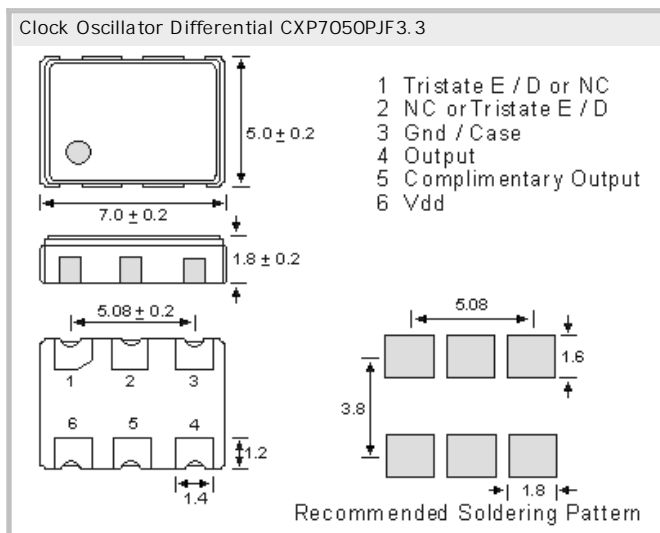
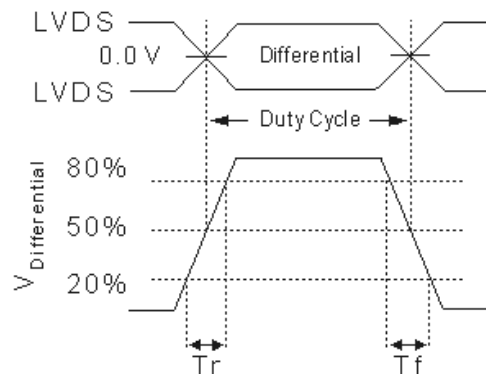


Clock Oscillator Differential CXP7050DJF3.3
LVDS 3.3V; ultra low jitter, with PLL

- SMD in ceramic case (7.0 x 5.0 x 1.8) mm
- Tri-State Enable / Disable on pad No. 1
- LVDS Differential Output Wave Form
- High Q fundamental crystal + ultra low jitter multiplier circuit
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies



LVDS Square Wave Output Wave Form



Specifications

Holder Type:	Clock Oscillator CXP7050DJF3.3 ; 3.3V(Voltage code is "3.3")
Frequency Range:	150 MHz to 2.100.0 MHz
Frequency Stability at 25°C:	± 25 ppm / ± 50 ppm
Operating Temperature Range:	± 25 ppm, -40°C to $+85^\circ\text{C}$ / ± 50 ppm, -40°C to $+85^\circ\text{C}$
Storage Temperature:	-55°C to $+125^\circ\text{C}$
Power Supply Voltage (Vdd):	+ 3.3V D.C. $\pm 10\%$
Maximum Supply Current (Differential):	100mA typ. 120mAmax.
Current with Output Disabled:	99 mA typical
Output Voltage (VOH) (VOL):	High "1" Vdd-1.165V min, Vdd- 0.8Vmax. Low "0" Vdd-2.0V min, Vdd- 1.55Vmax.
Start Up Time:	5ms typical; 10 ms max.
Output Symmetry (Duty Cycle):	50% $\pm 5\%$ max. (measured at 50% Vdd)
Load:	50 ohms into Vdd -2V or Thevenin equiv.
Rise (Tr) /Fall Time (Tf):	0.35ns typical; 0.5ns max. (20% Vdd \leftrightarrow 80% Vdd, 15pF load)
Phase Jitter:	0.15 ps typ. (12 kHz to 20 MHz); < 100 fs (1.875 MHz to 20MHz)
Phase Noise (156.250 MHz):	-67dBc/Hz @ 10Hz, -92dBc/Hz @ 100Hz, -112dBc/Hz @ 1kHz -121dBc/Hz @ 10kHz, -124dBc/Hz @ 100kHz, -136dBc/Hz @ 1MHz, -153dBc/Hz @ 5MHz
Aging:	< ± 2 ppm max. for the first year; ± 10 ppm max. over 10 years
Reflow Condition:	260°C max for 10 sec.

GERMANY:

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