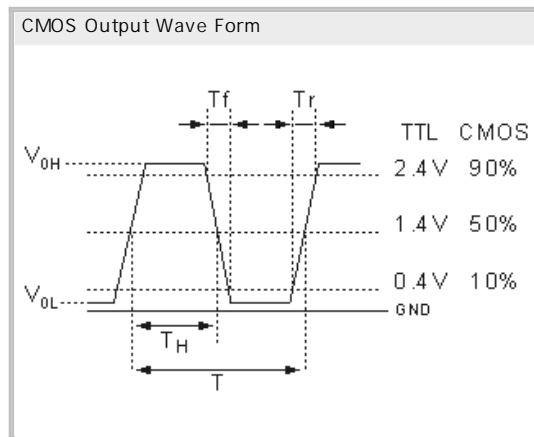
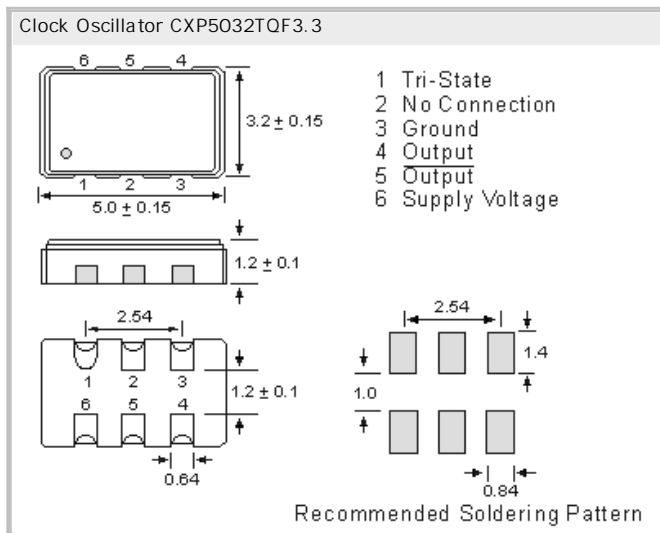




Clock Oscillator CXP5032TQF3.3  
LVCMOS/LVTTL 3.3V; ultra low jitter, with PLL

- SMD in ceramic case (5.0 x 3.2 x 1.2) mm
- Tri-State Enable / Disable on pad No. 1
- LVCMOS/LVTTL Square Wave Output Wave Form
- High Q fundamental crystal + ultra low jitter multiplier circuit
- RoHS conform; Lead-free product; on Tape (16mm) & Reel
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000G 1/2 sine wave
- Available in many standard and special frequencies



## Specifications

Holder Type:	CXP5032TSF3.3 ; 3.3V(Voltage code is "3.3"); Tri-State on pad 1
Frequency Range:	10 MHz to 245.0 MHz
Frequency Stability at 25°C:	$\pm 25$ ppm / $\pm 50$ ppm
Operating Temperature Range:	$\pm 25$ ppm, $-40^\circ\text{C}$ to $+85^\circ\text{C}$ / $\pm 50$ ppm, $-40^\circ\text{C}$ to $+85^\circ\text{C}$
Storage Temperature:	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Power Supply Voltage (Vdd):	+ 3.3V D.C. $\pm 10\%$
Maximum Supply Current (15pF load):	10 MHz 17 mA typical, 150MHz 28 mA 10 MHz 17 mA typical, 150MHz 28 mA
Current with Output:	16 mA typical
Output Logic Levels:	High "1" 90% of Vdd-min, Low "0" 10% Vdd-max.,
Start Up Time:	10 ms max.
Output Symmetry (Duty Cycle):	50% $\pm 2\%$ max. (measured at 50% Vdd)
Load:	15pF
Rise/Fall Time:	1.5ns typical; 3.0ns max. (10% Vdd $\leftrightarrow$ 90% Vdd, 15pF load)
Tri-state Function Pin 1 OE Control:	0.7% of Vdd min. or no connection to enable output. LVCMOS/LVTTL level. 0.3% of Vdd max. to disable output (high impedance). LVCMOS/LVTTL level.
Output Enable Time / Disable Time:	200 nS. Max. / 50 nS. Max.
Phase Jitter:	1.0 ps typ. (12 kHz to 20 MHz); < 100 fs (1.875 MHz to 20MHz)
Phase Noise (156.250 MHz):	-67dBc/Hz @ 10Hz, -92dBc/Hz @ 100Hz, -112dBc/Hz @ 1kHz -121dBc/Hz @ 10kHz, -124dBc/Hz @ 100kHz, -136dBc/Hz @ 1MHz, -153dBc/Hz @ 5MHz
Aging:	< $\pm 2$ ppm max. for the first year; $\pm 10$ ppm max. over 10 years
Reflow Condition:	260°C max for 10 sec.

### GERMANY:

COMTEC CRYSTALS GmbH · Sultenstrasse 12-14  
8 5 5 8 6 P o i n g / G E R M A N Y  
Phone +49 8121 778160 · Fax +49 8121 778177  
e-Mail [info@comtec-crystals.com](mailto:info@comtec-crystals.com)  
Internet: <http://www.comtec-crystals.com>  
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### FRANCE:

COMTEC CRYSTALS SARL · 23, rue du Faucon  
6 7 5 0 0 H a g u e n a u / F R A N C E  
Phone +33 388 732162 · Fax +33 388 730118  
e-Mail [sales@comtec-crystals.com](mailto:sales@comtec-crystals.com)  
Internet: <http://www.comtec-crystals.com>  
Sous réserve de modifications.