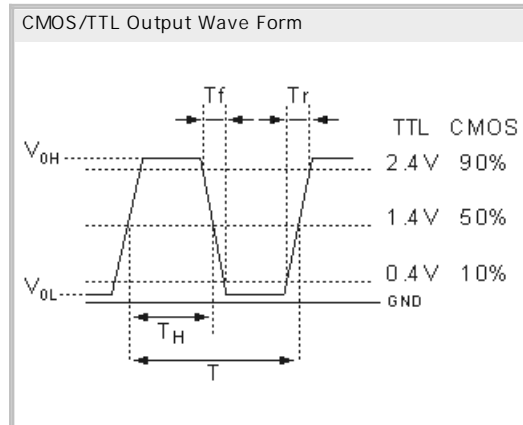
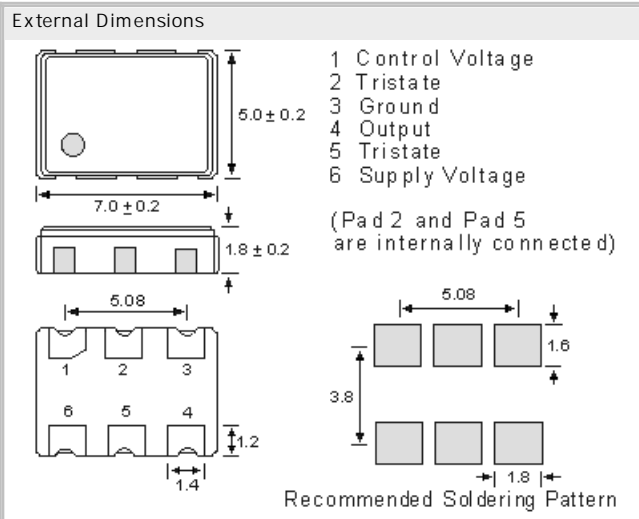


VCXO-Oscillator SMD VCXO7050T5.0-6pad, 5.0V Voltage Controlled Crystal Oscillator

- CMOS/TTL Output Wave Form
- SMD in ceramic case (7.0 x 5.0 x 1.8) mm, on Tape & Reel (Tape 16mm)
- with Tri-State Function, 3.3 V
- RoHS conform; Lead-free product
- Vibration: MIL-STD-202F method 204, 35G, 50 to 2000 Hz
- Shock: MIL-STD-202F method 213B, test cond. E, 1000GG 1/2 sine wave
- Available in many standard and special frequencies



## Specifications

|  |  |
|--|--|
| Holder Type:                             | VCXO7050T5.0-6pad 5.0V (Voltage code is " 5.0 " ) Tri-State  |
| Frequency:                               | 19.440000 MHz  |
| Initial Freq. Accuracy (at 25 °C):       | To tune to the nominal frequency with $V_c = 2.5V \pm 0.2V$  |
| Freq. Stability o.Operating Temp. Range: | $\pm 20.0$ ppm   |
| Operating Temperature Range:             | $\pm 20.0$ ppm over $-20^\circ C$ to $+70^\circ C$ (inclusive of $25^\circ C$ tolerance, $\pm 10\%$ input voltage variation, load change, aging, shock and vibration ) |
| Frequency Deviation:                     | $\pm 100$ ppm  |
| Power Supply Voltage (Vdd):              | + 5.0V DC $\pm 10\%$   |
| Maximum Supply Current:                  | 35.0 mA  |
| Output Load $C_L$ :                      | 2 TTL gates max. / CMOS 15 pF  |
| Output "1" Level (VOH):                  | 2.4V (min.) TTL / 4.5V (min.) CMOS   |
| Output "0" Level (VOL):                  | 0.4V (max.) TTL / 0.5V (max.) CMOS   |
| Output Symmetry (Duty Cycle):            | 40/60%   |
| Tri-State Function:                      | Tri-State Enable High. No connection or $V_{dd} - 0.5V_{min}$ . is applied to a Tri-state pin to enable output. Ground+0.5Vmax. to disable output (high impedance).    |
| Modulation Bandwidth (at -3 dB):         | 10KHz min, $V_{control}$ at 1.65V or at 2.5V   |
| Voltage Control:                         | 2.5V DC Center / 0.5V to 4.5V Range  |
| Linearity:                               | 6% typical; 10% max.   |
| Rise/Fall Time TTL:                      | 6ns (max.) 4ns (typ.) Measured between 0.4V and 2.4V   |
| Rise/Fall Time CMOS:                     | 6ns (max.) 4ns (typ.) Measured between 20% and 80% $V_{dd}$ of the wave form ( $C_L = 15pF$ )  |
| Integrated Phase Jitter:                 | 1 ps max. (12 kHz to 20 MHz)   |
| Period Jitter:                           | RMS 2.0 ps (typ.) / Peak to Peak 14 ps max.  |
| Phase Noise (27MHz at 3.3V):             | -40dBc/Hz at 10Hz; -104dBc/Hz at 100Hz ; -132dBc/Hz at 1kHz , -147dBc/Hz at 10kHz ; -152dBc/Hz at 100kHz ; -150dBc/Hz at 1MHz  |
| Start Up Time:                           | 10 ms (max.), 5ms (typ.)   |
| Aging:                                   | $\pm 3$ ppm per year (max.)  |
| Input Impedance:                         | 1 MOhm typical   |
| Reflow Condition:                        | 10 sec. max. at $260^\circ C$  |

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